DETAILED ACTION

Drawings

1. The drawings were received on 18 November 2002. These drawings are acceptable.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-6, 8-10, 13-17, 19, 21, 22, and 24-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Fee et al. (U.S. 5,485,576) hereinafter referred to as Fee.

a. Regarding claims 1 and 13, Fee teaches: powering the communication module (lines 26-30 of column 2); operating the communication module initially in a secondary status (lines 31-35 of column 2); broadcasting a request on the communication pathway for a response from a primary communication module (lines 35-41 of column 2); operating the communication module in a primary status if no response is received from the primary communication module (lines 35-41 of column 2); and broadcasting a message indicating the primary status (lines 61-65 of column 2).

b. Regarding claims 2 and 14, Fee teaches: starting a timer after the broadcasting a request step (lines 26-33 of column 4); monitoring the communication

pathway for a response from the primary communication module (lines 35-41 of column 2); and self promoting to the primary status if no response to the request is received before the timer reaches a predetermined time (lines 35-41 of column 2).

c. Regarding claims 3 and 15, Fee teaches: continuing to operate in the secondary status if a response is received from the primary communication module before the timer reaches a predetermined time (lines 31-35 of column 2).

d. Regarding claim 4, Fee teaches: a first communication module (lines 26-30 of column 2); a second communication module (lines 26-30 of column 2); a first communication pathway coupling the first communication module and the second communication module (lines 26-30 of column 2); and wherein each of the first and second communication modules are adapted to initially assume a secondary status, request a response from a primary communication module, self promote to primary status if no response is received, and if applicable, broadcast the primary status across the first communication pathway (lines 31-41 of column 2).

e. Regarding claims 5 and 6, Fee teaches: wherein the first and second communication modules are power supplies communication module in a rack of servers (lines 50-64 of column 3 and Fig. 1).

f. Regarding claim 8, Fee teaches: a third communication module coupled to the first and second communication modules through the first communication pathway (lines 42-50 of column 2); wherein the third communication module monitors the first communication pathway to ascertain which of the first and second communication modules is primary (lines 4250 of column 2); and wherein the third communication

module directs communications one of the first and second communication modules that has taken the primary status (lines 53-65 of column 2).

g. Regarding claims 9 and 10, Fee teaches: the first and second communication modules are power supply communication modules adapted to monitor a power supply assembly of a power supply system in a rack of servers (lines 26-41 of column 2).

h. Regarding claim 16, Fee teaches: a random access memory (RAM) device (item 30 of Fig. 2); a read only memory (ROM) device (items 82 and 86 of Fig. 2); a processor coupled to the RAM and ROM devices (item 70 of Fig. 2); a first communication pathway coupled to the processors (item 90 of Fig. 2); a second communication pathway coupled to the processor (item 88 of Fig. 2); wherein the processor is adapted to execute programs stored on the ROM device (lines 33-38 of column 5); and wherein the programs stored on the ROM device direct the communication module to default to a secondary status for control of the first communication pathway (lines 31-35 of column 2), and wherein the programs further direct the processor to request a response from a primary communication module across the first communication pathway, self-promote to a primary status if no response is received, and broadcast the primary status across the first communication pathway (lines 31-41 of column 2).

i. Regarding claim 17, Fee teaches: wherein the processor further comprises a microcontroller (item 28 of Fig. 1).

j. Regarding claim 19, Fee teaches: the first communication pathway is a serial communication pathway (lines 18-22 of column 4).

k. Regarding claim 21, Fee teaches: wherein the ROM devices is an EEPROM (item 82 of Fig. 2).

l. Regarding claim 22, Fee teaches: the programs stored on the ROM device executed by the processor further direct the communication module to remain in the secondary status if a response is received from the primary communication module (lines 26-33 of column 4).

m. Regarding claim 24 Fee teaches: powering the communication module (lines 26-30 of column 2); operating the communication module initially in a secondary status (lines 31-35 of column 2); broadcasting a request on the communication pathway for a response from a primary communication module (lines 35-41 of column 2); operating the communication module in a primary status if no response is received from the primary communication module (lines 35-41 of column 2); and broadcasting a message indicating the primary status (lines 61-65 of column 2); starting a timer after the broadcasting a request step (lines 26-33 of column 4); monitoring the communication pathway for a response from the primary communication module (lines 35-41 of column 2); and self promoting to the primary status if no response to the request is received before the timer reaches a predetermined time (lines 35-41 of column 2); and operating all but the first of the communication modules in a secondary status (lines 35-41 of column 2).

n. Regarding claim 25, Fee teaches: choosing a primary communication module among communication modules whose timers expire substantially simultaneously based on device addresses for each of the communications modules whose timers expire substantially simultaneously (lines 26-33 of column 4).

o. Regarding claim 26, Fee teaches: choosing a primary based on device addresses further comprises choosing one of the communication modules whose timers expired simultaneously having the highest device address (lines 26-33 of column 4).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 7, 11, 12, 18, 20, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fee as applied to claims 6 and 10 above, in view of what was well known in the art at the time of the applicant's invention.

a. Regarding claims 7, 11, and 20, Fee does not explicitly teach: wherein the first communication pathway is an RS-485 communication pathway. However, Official Notice is taken of the RS-485 communication pathway. Now known as EIA-485, this standard has been in use for many years (invented in the 1960's) and has been used for communication between two devices. It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to use RS-485 as the first

communication pathway. The RS-485 is a two-wire, half-duplex, multipoint serial connection which has been in use for years. It is for this reason that one of ordinary skill in the art at the time of the applicant's invention would have been motivated to use RS-485 as the first communication pathway in the system as taught by Fee.

b. Regarding claim 12, Fee teaches: the third communication module is a chassis communication module adapted to communicate on behalf of servers within a particular chassis in a rack of servers (lines 53-65 of column 2).

c. Regarding claim 18, Fee does not explicitly teach: wherein the microcontroller further comprises a Zircon-ZH2 manufactured by Qlogic Corporation. However, Official Notice is taken of the Zircon-ZH2 microcontroller. Use of the ZH2 microcontroller is merely design choice and could be replaced by any number of microcontrollers. The applicants have provided no reasoning and/or advantages for using this specific microcontroller. Therefore, the type of microcontroller used is completely arbitrary. It is for this reason that one of ordinary skill in the art at the time of the applicant's invention would have been motivated to use a Zicron-ZH2 microcontroller in the system as taught by Fee.

d. Regarding claim 23, Fee teaches: wherein the second communication pathway comprises an I2C serial communication pathway. However, Official Notice is taken of the I2C communication pathway. This standard has been in use for many years (invented in the 1980's) and has been used for communication between two devices. It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to use I2C as the second communication pathway. The I2C is a

two-wire, low-bandwidth, short distance protocol which has been in use for years. It is for this reason that one of ordinary skill in the art at the time of the applicant's invention would have been motivated to use I2C as the second communication pathway in the system as taught by Fee

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Meucci at (571) 272-3892. The examiner can normally be reached on Monday-Friday from 9:00 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Caldwell, can be reached at (571) 272-3868. The fax phone number for this Group is 571-273-8300.

Communications via Internet e-mail regarding this application, other than those under 35 U.S.C. 132 or which otherwise require a signature, may be used by the applicant and should be addressed to [michael.meucci@uspto.gov].

All Internet e-mail communications will be made of record in the application file. PTO employees do not engage in Internet communications where there exists a possibility that sensitive information could be identified or exchanged unless the record includes a properly signed express waiver of the confidentiality requirements of 35 U.S.C. 122. This is more clearly set forth in the Interim Internet Usage Policy published in the Official Gazette of the Patent and Trademark on February 25, 1997 at 1195 OG 89.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Andrew Caldwell/
Supervisory Patent Examiner, Art Unit 2142